Revised Edition

ADVANCED COMPUTER ARCHITECTURE

(A Practical Approach)

• Parallel Algorithms • Parallel Programming • Super Computers

Er. RAJIV CHOPRA

S. CHAND

ADVANCED COMPUTER ARCHITECTURE

(A Practical Approach)

• Parallel Algorithms • Parallel Programming • Super Computers

For :

- B. Tech. (CSE)–7th sem., GGSIPU.
- M. Tech (CSE)–1st sem., GGSIPU.
- B. Tech (CSE)–7th & 8th sem., UPTU.
- B. Tech (CSE)–5th sem., Pune Univ.
- MCA (SE)–5th sem., GGSIPU.
- B. Tech (IT)–7th & 8th sem., UPTU.
- M. Tech (CSE)–1st sem., P.T.U.
- B.E. (CSE)–7th sem., KUD.

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PREFACE TO THE THIRD EDITION

Many books on Advanced Computer Architecture are available in the market but they are not complete, are very formal and dry. My attempt is to make ACA very simple so that a student feels as if the teacher is sitting behind him and guiding him. This text is bolstered with many examples and CASE STUDIES. Also included in this text are the experiments to be performed in ACA lab. Every effort has been made to alleviate the treatment of the book for easy flow of understanding of the students as well as the professors alike.

Any suggestions to further enhance the quality of the book will be highly acknowledged.

Er. RAJIV CHOPRA
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Writing a good book not only requires sincere efforts and hard work but also the blessings of the omnipresent GOD. I thank the support given by S. Bhatnagar, Mr. Madan, his colleagues and the entire team of S. Chand for publishing this book in a nice format. I also acknowledge the support given by my parents-DR. J. R. CHOPRA (Ex-Professor of Physics) and Mrs. Sushma Chopra (Ex-Principal) during the writing of this book. Lastly, I acknowledge my twin babies- Arjeesh (son) and Arshitha (daughter) and my wife Shakti Chopra for their patience and motivations.

Er. Rajiv Chopra

Syllabus of GGSIPU

Code No. : ETCS 403 **L T C**

Paper : Advanced Computer Architecture (B. Tech. – CSE) **3 1 4**

INSTRUCTION TO PAPER SETTERS :

1. Questions No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 25 marks.
2. Apart from question no. 1. rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 questions from each unit. Each question should be of 12.5 marks.

UNIT - I

1. **Parallel computer models :** The state of computing, Multiprocessors and multicomputers, Multivector and SIMD computers, Architectural development tracks.
2. **Program and network properties :** Conditions of parallelism, Data and resource dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain size and latency, Program flow mechanisms, Control flow versus data flow, Data flow architecture, Demand driven mechanisms, Comparisons of flow mechanisms

[No. of Hrs.: 11]

UNIT - II

3. **System Interconnect Architectures :** Network properties and routing, Static interconnection networks, Dynamic interconnection Networks, Multiprocessor system interconnects, Hierarchical bus systems, Crossbar switch and multiport memeory, Multistage and combining network.
4. **Processors and Memory Hierarchy :** Advanced processor technology, Instruction-set Architecture, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors.
5. **Memory Technology :** Hierarchical memory technology, Inclusion, Coherence and Locality, Memory capacity planning, Virtual Memory Technology. **[No. of Hrs .: 11]**

UNIT - III

6. **Backplane Bus System :** Backplane bus specification, Addressing and timing protocols, Arbitration transaction and interrput, Cache addressing models, Direct mapping and associative caches.
7. **Pipelining :** Linear pipeline processor, Nonlinear pipeline processor, Instruction pipeline design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch handling techniques, Arithmetaic Pipeline Design, Computer arithmetic principles, Static arithmetic pipeline, Multifunctional arithmetic pipelines. **[No. of Hrs. 11]**

UNIT - IV

8. **Vector Processing Principles :** Vector instruction types, Vector-access memory schemes.
9. **Synchronous Parallel Processing :** SIMD Architecture and Programming Principles, SIMD Parallel Algorithms, SIMD Computers and Performance Enhancement.

[No. of Hrs. : 11]

ACADEMIC PLAN FOR VII SEMESTER (FOR YEAR 2008-09)

[GGSIPU, DELHI]

SUBJECT : ADVANCED COMPUTER ARCHITECTURE **Subject Code : ETCS 403**

Branch . B. Tech. (CSE) ; 7th Sem. **Total Lectures : 42**

Total Tutorials : 14

Total teaching weeks in semester : 14 weeks

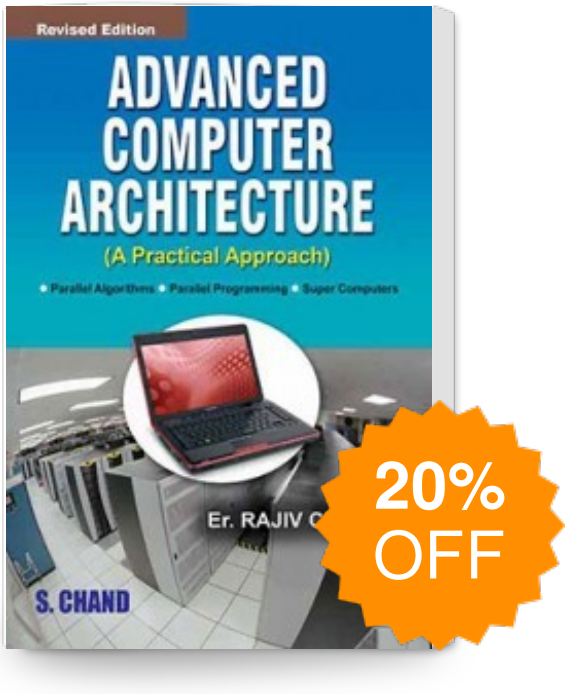
	TOPICS TO BE COVERED	Total No. of Lecture/Tutorial	
	First Term	**Lecture**	**Tutorial**
	Parallel computer models		
1.	The state of computing	1	
2.	Multiprocessors and multi-computers	1	
3.	Multi-vector and SIMD computers, Architectural development tracks	1	1
	Program and network properties		
4.	Conditions of Parallelism Data and resource dependencies.	1	
5.	Hardware and software parallelism	2	1
6.	Program partitioning and scheduling, Grain size and latency	1	
7.	Program flow mechanisms	1	
8.	Control flow versus data flow, Demand driven mechanisms	1	1
9.	Data flow architecture	2	
10.	Comparisons of flow mechanisms	1	1
	System Interconnect Architectures		
11.	Network properties and routing, Static interconnection networks	1	
12.	Dynamic interconnection Networks	2	1
13.	Multiprocessor system interconnects, Hierarchical bus systems, Crossbar switch and multi-port memory, Multistage and combining network.	3	1
	Second Term		
	Processors and Memory Hierarchy		
14.	Advanced processor technology, Instruction-set Architectures	1	
15.	CISC Scalar Processors, RISC Scalar Processors	1	
16.	Superscalar Processors, VLIW Architectures	2	1
17.	Vector and Symbolic processors	1	
	Memory Technology		
18.	Hierarchical memory technology, Inclusion Coherence and Locality, Memory capacity planning	2	1
19.	Virtual Memory Technology	2	1

	Back plane Bus System :		
20.	Back plane bus specification, Addressing and timing protocols	1	
21.	Arbitration transaction and interrupt	1	1
22.	Cache addressing models, Direct mapping and associative caches	1	
	Pipelining		
23.	Linear pipeline processor	1	
24.	Nonlinear pipeline processor	1	1
25.	Instruction pipeline design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch handling techniques	2	
26.	Arithmetic Pipeline Design, Computer arithmetic principles, Static arithmetic pipeline, Multifunctional arithmetic pipelines	2	1
	Third Term		
	Vector Processing Principles		
27.	Vector instruction types	1	
28.	Vector-access memory schemes	1	1
	Synchronous Parallel Processing		
29.	SIMD Architecture and Programming Principles, SIMD Parallel Algorithms	2	1
30.	SIMD Computers and Performance Enhancement	1	

CONTENTS

UNIT - I

Advanced Computer Architecture



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