VLSI Circuits

Notes

ELEMENTS OF PHYSICAL DESIGN

3.1 Introduction to Physical Design

Several equivalent viewpoints may be used to describe an integrated circuit. To a circuit designer, a chip is the physical realization of an electronic network. A logic designer, on the other hand, may choose to view the chip as a device that performs functions specified by logic diagrams, function tables, or an HDL file. Figure 3.1 illustrates how different people might view the same thing. Regardless of the abstraction used, in the final analysis, an integrated circuit is really an intricate physical object that has been carefully designed and fabricated.

Physical design in VLSI deals with the procedure needed to realize a circuit on the surface of a semiconductor wafer. Starting with the electrical network schematic, computer tools are used to create the necessary patterns on each layer in the 3-dimensional structure. Once the drawings are completed, the information can be used to fabricate the masks needed in the processing line.

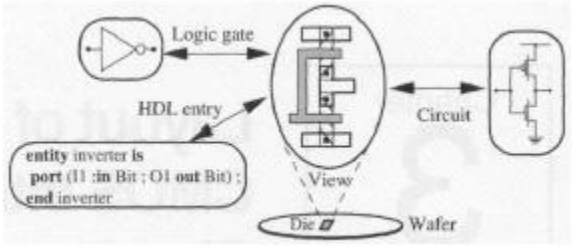

Figure 3.1. Equivalent descriptions of a digital integrated circuit.

CMOS technology allows one to choose from a wide variety of circuit design techniques, any of which may be useful when implementing a given logic function. This feature is particularly nice when designing high-performance circuits, as often one design style yields faster switching than another. Physical design is critical in this situation, since the layout and the resulting performance are directly linked to each other. At this level, the circuit design and layout are indistinguishable.

Many people view physical design as a skill that is best learned by doing. The most proficient designers tend to be the most experienced, but, of course, one must begin somewhere. In this chapter, we will introduce the first ideas of physical design by examining the concept of layout in more detail. This includes ideas such as design rules and interconnect routing. The details of designing CMOS circuits will be covered in the following chapters.

3.2 Masks and Layout Drawings

Every material layer in an integrated circuit is described by a set of geometrical objects of specified shape and size. These objects are defined with respect to each other on the same layer, and also with reference to geometrical objects that lie on other layers, both above and below. Layout drawings relay this information graphically, and can be used to generate the masks needed in the fabrication process.

Because of this relationship, we will take the viewpoint that a layout drawing represents the top view of the chip itself.

When we visualize an integrated circuit, it appears as a set of overlapping geometrical objects. In a layout editor, each layer is described by using a distinct color or fill pattern that allows us to see the objects relative to each other. Once we get oriented to seeing an integrated circuit in this manner, it is a simple matter to construct transistors and route the interconnect lines as required. While classical schematic representations provide the topology of the network, the layout gives us the ability to modify the performance of a circuit. Performing the layout is therefore an intrinsic part of the design process.

When designing digital logic circuits in CMOS, the goals remain quite simple:
• Design a circuit that implements the logic function correctly, and,
• Adjust the parameters to meet the electrical specifications.
This is often more difficult than it sounds, particularly when we note that state-ofthe art VLSI chips can have several million MOSFETs with the associated interconnect lines. At the most basic level, we find that many problems arise when performing the layout of an integrated circuit. Some deal with the practical aspects of circuit operation, others originate from physical properties of the materials involved, and yet others are due to limitations in the fabrication processes. These all contribute to the techniques used in the physical design.

3.3 Design Rule Basics

Design rules are a set of guidelines that specify the minimum dimensions and spacings allowed in a layout drawing. They are derived from constraints imposed by the processing and other physical considerations. Violating a design rule may result in a non-functional circuit , so that they are crucially important to enhancing the die yield.
Limitations in the photolithography and pattern definition give rise to several critical design rules. Since these are strongly dependent on equipment used in the fabrication process, they tend to change with improving technology. The situation is complicated by the fact that physical phenomena and device design considerations also enter into the picture. In this section, we will examine some of the

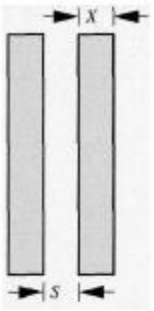

Figure 3.2. Minimum width and spacing.

design rules associated with a CMOS processing technology.

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3.3.1 Minimum Linewidths and Spacings

Consider the two objects shown in Figure 3.2. These represent two patterns on the same layer, e.g., both are polysilicon. When used as interconnects, the two rectangles shown in the drawing are called "lines" (since every physical patterning must have a non-zero width), and we will use this terminology in our discussion. The **minimum linewidth** *X* is the smallest dimension permitted for any object in the layout drawing; *X* is also known as the **minimum feature size. The minimum spacing** *S* is the smallest distance permitted between the edges of two objects; in the present example, the minimum spacing is between the two lines.
Minimum linewidth and spacing values for interconnect lines may originate from the resolution of the optical printing system, the etching process, or from other considerations such as surface roughness. Violating the minimum linewidth rule may result in ill-defined or broken interconnects. Similarly, the minimum spacing rule ensures that the lines are physically separated in the final structure. If this guideline is not followed, then the two may form an electrical short in the circuit. The situation is more complicated when applied to patterning a doped region in

the silicon because of lateral doping effects and the presence of depletion regions. Lateral doping is shown in Figure 3.3. In (a), the oxide has been patterned by the lithography to have a linewidth *X*. However, when the wafer is heated to anneal the implant, lateral diffusion[2] increases the actual width of the n^+ region to $X'>X$. This
Note that even a single defect results in a non-functioning circuit.

(a) Mask definition (b) After annealing

Figure 3.3. Patterning sequence for a doped n^+ line.

effect is important when determining the minimum spacing 5 between adjacent doped lines.

Depletion effects also influence the value of 5. As shown in Figure 3.4, a depletion region exists at every pn junction. Let us assume for simplicity that the junction has a step-doping profile where the impurity concentration changes abruptly from N_d on the n-side to N_a on the p-side. With a reverse-bias voltage of V_K, the total depletion width x_d can be computed from

$$x_d = x_0\sqrt{1+\frac{V_R}{V_{bi}}}, \qquad (3.1)$$

where

$$x_0 = \sqrt{\frac{2\varepsilon_{Si}V_{bi}}{q}\left(\frac{1}{N_a}+\frac{1}{N_d}\right)} \qquad (3.2)$$

is the zero-bias value of the total depletion width, and

(3-3)

is the built-in voltage. Table 3.1 provides a list of useful numerical values for basic calculations. Note that the intrinsic concentration n_i applies only to silicon at room temperature (T=300° *K).* To calculate the p-side depletion width x_p shown in the drawing, we use

$$x_p = \left(\frac{N_d}{N_d+N_a}\right)x_0\sqrt{1+\frac{V_R}{V_{bi}}}. \qquad (3.4)$$

Since this increases with the reverse bias voltage, the minimum spacing distance 5 often accounts for the worst-case situation, i.e., when $V_R=V_{DD}$. From this discussion, it is not surprising that the minimum width and spacing for n^+ and p^+ regions are usually larger than those for a polysilicon line.

3.3.2 Contacts and Vias

Contacts and vias are used to provide electrical connections between different material layers. In general, contacts are necessary connections to access the various regions of silicon, while vias are used between two interconnect layers to simplify the layout. When formulating design rules for these types of objects, two important considerations arise: the physical size of the oxide cuts, and the spacing needed around the connection on the layers.

TABLE 3.1 Useful constants

Symbol	Parameter name	Value	Units
	Electron charge	1.6 x10^{-19}	Coulombs
$\varepsilon_S=\varepsilon_r\varepsilon_0$	Permittivity of silicon	(11.8)(8.854x 10^{-14})	Farads/cm
	Permittivity of SiO_2	(3.9X8.854 x10^{-14}	Farads/cm
n_i	Intrinsic concentration	1.45x10^{10}	cm^{-3}
(kT/q)	Thermal voltage	0.0258	Volts

Let us first examine the dimensions of a contact region. The geometry is shown in Figure 3.5. It is apparent that the minimum size is limited by the lithographic process. However, this does not imply that one uses the largest contacts possible, as other considerations come into play. If the contact cut is too large, then it may be difficult to attain complete coverage when depositing the upper layer. Large contact cuts may result in cracks or voids, that may in turn lead to a circuit failure. To overcome this problem, it is common to restrict the dimensions of contact cuts to prespecified values that can be reliably made in the fabrication process.

Now, consider the problem of spacing *x* around an oxide cut as shown in Figure 3.6. We must specify the minimum distance between the edge of an oxide cut and the edge of a patterned region to allow for misalignment tolerances in the masking steps. These are generically classified as **registration errors,** and arise because it is not possible to align the mask with arbitrary precision.

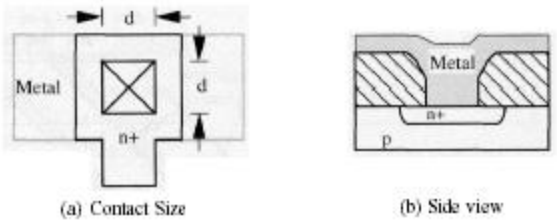


Figure 3.5. Geometry of a contact cut.

3.3.3 MOSFET Rules

MOSFETs are usually fabricated using the self-aligned technique described in the last chapter. This approach uses the polysilicon gate as a mask for the ion implantation step that forms the drain/source regions. Certain precautions must be taken in the physical design to ensure that small registration errors can be tolerated, and functional transistors will still be formed.

First, we recall that n^+ regions in an nFET are described by the derived layer[1] ndiff = (ACTIVE) AND (NSELECT).

With regard to the fabrication sequence, this means that an n^+ region is formed where (a) the NSELECT mask gives an opening in the photoresist, AND, (b) an ACTIVE area exists to allow the implant to penetrate into the silicon substrate. Since the formation of the physical ndiff layer relies on the overlap of two masks, the size of the NSELECT region must be larger than the size of the corresponding ACTIVE area.

The drawing in Figure 3.7(a) shows the proper sizing of the two layers, with the NSELECT rectangle larger than the ACTIVE area rectangle. The final dimensions of the n^+ region are those of the ACTIVE area. A minimum spacing value *x* between the edges of the two masks is used to allow for registration error between

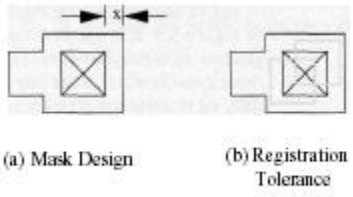


Figure 3.6. Contact spacing rule.

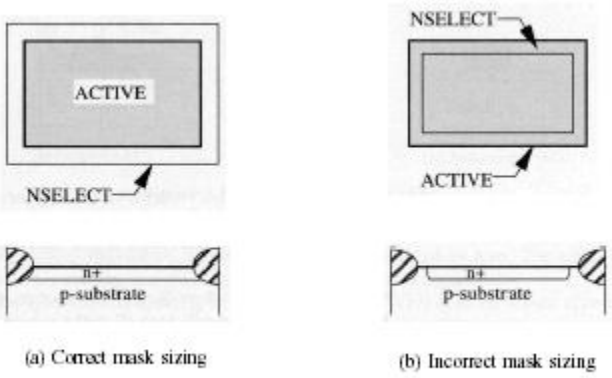


Figure 3.7. Formation of n+ regions in an n-channel MOSFET

the two masks. Even though the ion implant specified by the NSELECT boundary is larger than needed, the thick field oxide specified by the region NOT(ACTIVE) prevents the underlying silicon from being doped. This is verified by the cross-sectional view shown.

If we reverse the situation and make the ACTIVE area larger than the NSELECT area, then only the region described by ndiff=(ACTIVE) AND (NSELECT) will become n_+; sections corresponding to

(ACTIVE) AND [NOT(NSELECT)]

remain p-type substrate. This is shown in Figure 3.7(b). The ndiff region does not have the correct cross-sectional pattern needed to ensure proper isolation and operation.

Consider next the **gate overhang** distance *d* shown in Figure 3.8. This is included to ensure that a misaligned gate will still yield a structure that has separate drain and source regions. To understand the reasoning, suppose that a MOSFET is designed using the layout shown in Figure 3.9(a) with *d=0.* Figure 3.9(b) shows a

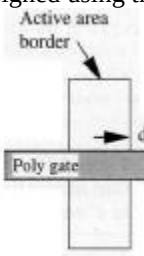


Figure 3.8.
Gate overhang in MOSFET layout.

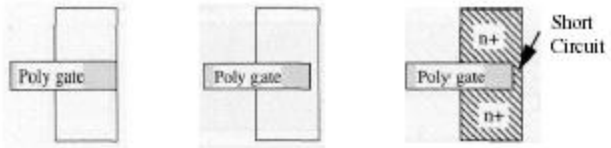


Figure 3.9. Effect of gate misalignment without overhang.

small misalignment where the polysilicon does not traverse the entire active area. Since the ion implant will dope all of the exposed substrate, the resulting structure shown in (c) has the drain and source n_+ regions merged into one. Electrically, the drain and source are shorted, so the device cannot control the current flow, i.e., the switching action has been lost.

The same consideration applies to a MOSFET where the n+ region changes shape as shown in Figure 3.10. The channel width W is a critical design parameter, so that the spacing *s* between the poly and n_+-edges must be large enough to ensure that the MOSFET still has the proper value if small registration errors occur.

3.3.4 Bloats and Shrinks

The drawings produced by a layout editor provide the basic view of an integrated

circuit that are used to extract the equivalent device parameters. It is therefore important to understand the correlation between what is shown on the computer monitor when compared with the actual die after fabrication.
In general, the final size of a physical layer will be different from the dimensions specified by the mask that created the pattern. Two obvious examples are
• ACTIVE: Encroachment reduces the size of the usable active area.
• Doped n^+ or p^+: Lateral doping effects increase the size of these regions.
In addition, the physical process of etching a material layer is anisotropic, with both vertical and lateral etching present. Although the lateral etch rate can be reduced

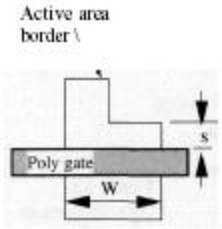


Figure 3.10. Gate spacing from an n^+ edge.

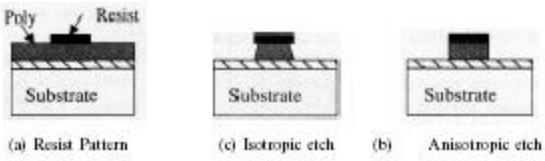


Figure 3.11. Polysilicon etch profiles.

using various techniques, it cannot in general be reduced to zero. The effect of anisotropic etching on a polysilicon layer is illustrated in Figure 3.11.
The question that naturally arises at this point is "What does the layout drawing represent relative to the finished chip?" In other words, will the chip patterns be identical to those shown by the layout editor, or are size adjustments necessary? In the early days of chip design, one had to increase or decrease the size of the layout drawing to view the actual chip dimensions. However, it is now common for the chip fabricator to subject the masks to bloats (increases in object sizes) and shrinks (decreases in the object size) as needed to compensate for the difference between the mask dimensions and the resulting size on the chip. When this is done, then the layout editor displays a reasonably accurate view of the finished circuit.
These considerations are particularly important to designing a MOSFET. Although the two critical dimensions L (the channel length) and W (the channel width) are related to the **drawn** mask values, the values are different as shown in Figure 3.12. The channel length L that is required in the current flow equations is reduced from the drawn value L' by

$$L = L - 2L \quad \textbf{(3.5)}$$

where L_0 is the overlap distance from lateral diffusion effects . In a similar manner, the channel width W is smaller than the drawn ACTIVE width W because of active area **encroachment.** This is where the usable size of the active area is reduced because of oxide growth underneath the edges of the nitride pattern. If the encroachment per side is (AW), then

$$W = W-2(\Delta W) \quad \textbf{(3.6)}$$

gives the proper electrical value. This can become confusing when entering the device dimension into a circuit simulation program. For example, SPICE parameters can be entered using either the drawn or physical values so long as the remaining data values are consistent. This will be discussed in more detail in the next chapter.
The gate overlap L_0 is also known as the lateral diffusion length L_D.

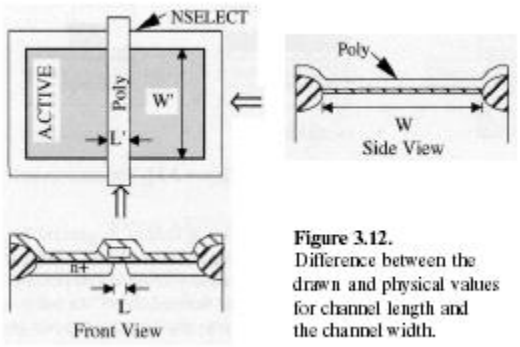


Figure 3.12.
Difference between the drawn and physical values for channel length and the channel width.

3.4 Types of Design Rules

Geometrical design rules are a set of minimum widths, spacings, and layout guidelines needed to create the masks. There are two ways to specify these dimensions:

• **Specific Values:** All dimensions are stated in standard unit of length, such as the micron;

• **Scalable:** Distances are specified as multiples of a metric λ, that has dimensions of length. The actual value of λ, is adjusted to correspond to the limitations of the process line.

Both approaches are common in CMOS VLSI. Scalable rules have the advantage that they can be adjusted to several different processing lines by changing the value of **λ**. However, this does not come without cost. Since every distance is specified as a multiple of **λ**, the numerical value is dictated by the worst-case situation. This generally decreases the compaction density of the circuit compared to what is attainable if the parameters are specified in an absolute metric such as microns.

In general, there are three main classes of design rule specifications. These are

• Minimum Width,

• Minimum Spacing, and,

• Surround.

Surround rules apply to objects placed within larger objects (such as contacts). Every layer has a minimum width and minimum spacing value, while surrounds are specified as required.

3.5 CMOS Design Rules

In this section, we will examine a basic set of CMOS design rules to understand the presentation and meaning of each type of rule. This set has been provided in the setup technology file as **ledit.tdb,** and is also available with the name **morbn20.tdb.** The DR set describes the MOSIS Orbit 2-micron double-poly, double-metal, n-well CMOS process; the technology name for this process is SCNA (for Scalable CMOS N-Well Analog). For the purposes of this discussion, we will not list all layers. In particular, the POLY2 layer is not shown explicitly here to simplify the discussion.

A complete design rule set contains all of the geometric limits for mask layout. This includes the minimum feature sizes and minimum spacings on each mask, and also provides layer-to-layer spacings when necessary. In order to list the rules in an easy-to-find format, they are presented according to the order of the masks used in the processing. The primary design rule layers for the morbn20 technology are listed in Table 3.2.

TABLE 3.2 SCNA Design Rule Layers

Mask Number	Mask Layer
1.	NWELL
2.	ACTIVE
3.	POLY
4.	SELECT
5.	POLY CONTACT
6.	ACTIVE CONTACT
7.	METAL1
8.	VIA
9.	METAL2
10.	PAD
11.	POLY2

When you are using L-Edit, the design rules corresponding to the technology are always loaded into your file, and are Saved when you save your work. A text listing of the design rules can be obtained using the keyboard command Alt-W; there is no Menu Bar equivalent. This action writes a text file named **filename.rul** to the working disk drive that provides a listing of all layers and rules in ASCII format. The list also provides information on derived layers.

Design rule sets are most easily understood by providing a text list in conjunction with simple drawings to illustrate each value. These are broken into groups corresponding to each basic layer. The layer number N. is used to identify the group, and each dimensional specification is labelled accordingly, e.g., N.1, N.2, and so on. In order to clarify some of the fine points involved with design rules, they will be presented in two different forms. First, we will examine a simplified set of rules that provide basic information on minimum widths and spacings, and then look at MOSFET layout rules. This gives a general idea of what the rules mean. This is followed by a more complete set of layout statements that correspond to those used by L-Edit in performing the DRC algorithm.

3.5.1 Basic Rules

The most fundamental layout guidelines limit the smallness of each material layer, and provide the basis for device design. The values in this design rule set are scalable according to the metric λ Numerically, λ= 1 μm for the 2 μm technology.

However, these rules also apply to the mhp_n12.tdb (named SCN) 1.2-micron, single-poly, double-metal process with a metric of value λ= 0.6 μm.

Minimum Widths and Spacings

This group of rules are those that specify the minimum linewidths and minimum spacings permitted on the primary layers summarized in Table 3.3 and illustrated in Figure 3.13.

TABLE 3.3 Minimum Width and Spacing Rules

Layer	Type of Rule	Value
POLY	Minimum width	2λ
	Minimum spacing	2λ
ACTIVE	Minimum width	3λ
	Minimum spacing	3λ
NSELECT	Minimum width	3λ
	Minimum spacing	3λ
METAL1	Minimum width	3λ
	Minimum spacing	3λ
METAL2	Minimum width	3λ
	Minimum spacing	4λ

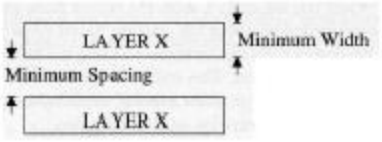


Figure 3.13 Minimum width and minimum spacing.

MOSFET Layout

The basic layout rules for MOSFETs are illustrated in Figure 3.14, and the values are summarized in Table 3.4. Dimensions that deal with POLY and N+/P+ apply equally to both nFETs and pFETs. Contacts (cuts in the oxide that allow electrical connections between two layers) to N+/P+ are called ACTIVE CONTACTS, while POLY CONTACTS provide access to the POLY layer (which must be in field regions).

In this technology, p-channel MOSFETs must be inside n-well regions, and sufficient spacing must be provided between opposite-polarity regions (i.e., between n_+ and p_+ sections) as well as between P+ regions and the NWELL edge. Spacing requirements also apply between different n-well regions; in general, a larger space is needed if the n-wells are biased at different voltages, due to the voltage dependence of depletion regions.

TABLE 3.4 MOSFET Layout Rules

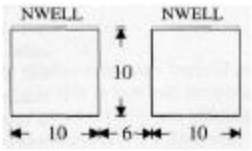
RULE	Meaning	Value
POLY Overlap	Minimum extension over ACTIVE	
POLY-ACTIVE	Minimum Spacing	3λ
MOSFET Width	Minimum N+/P+ MOSFET W	3λ
ACTIVE CONTACT	Exact Size	2λx2λ
ACTIVE CONTACT	Minimum Space to ACTIVE Edge	2λ
POLY CONTACT	Exact Size	2λx2λ
POLY CONTACT	Minimum Space to POLY Edge	1λ

3.5.2 Mask-Based Design Rule Set

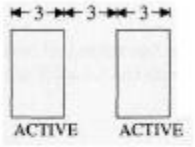
At the layout level, design rules apply to the masks involved in the chip patterning process. L-Edit employs a complete set of rules that apply to both masking layers and derived layers. Using derived layers allows us to make the connection between the individual patterns and the material layers that are important to the operation of transistors and other devices.

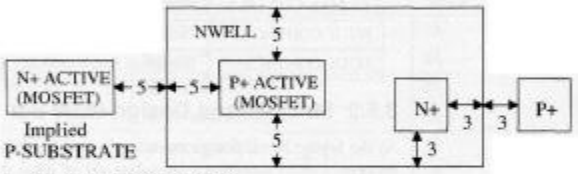
Figures 3.15, 3.16, and 3.17 provide most of the SCNA design rule set using

1.0 NWELL
- 1.1 Minimum Width 10
- 1.3 Minimum Spacing 6



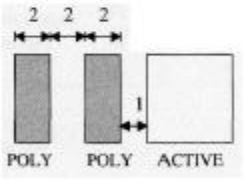
2.0 ACTIVE (N+, P+)
- 2.1 Minimum Width 3
- 2.2 Minimum Spacing 3
- 2.3 Drain/Source ACTIVE to NWELL
  - 2.3a P+ ACTIVE to NWELL . . . 5
  - 2.3b N+ACTIVE to NWELL . . . 5
- 2.4 CONTACT to NWELL EDGE
  - 2.4a P+ in SUB to NWELL . . . 3
  - 2.4b N+in WELL to NWELL . . 3





N+ = (NSELECT) AND (ACTIVE)
P+ =(PSELECT) AND (ACTIVE)

3.0 POLY
- 3.1 Minimum Width 2
- 3.2 Minimum Spacing 2
- 3.3 Gate Extension out of ACTIVE . 2
- 3.4 Extension (MOSFET)
  - 3.4a nMOSFET Drain/Source . . . 3
  - 3.4b pMOSFET Drain/Source . . . 3
- 3.5 POLY to ACTIVE Spacing . . . 1



N+ = (NSELECT) AND (ACTIVE)
P+ = (PSELECT) AND (ACTIVE)

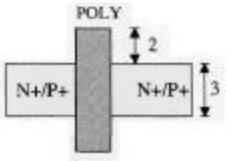
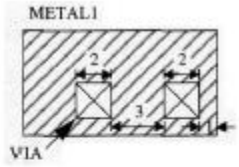


Figure 3.15. SCNA design rules.

8.0 VIA
- 8.1 Exact Size . . . . . 2 x 2
- 8.2 VIA to VIA Spacing 3
- 8.3 METAL1 Overlap of VIA . . 1
- 8.4 VIA Spacing
  - 8.4a VIA to POLY 2
  - 8.4b VIA (on POLY) to POLY . . 2
  - 8.4c VIA to ACTIVE 2
  - 8.4b VIA (on ACTIVE) to POLY . 2



9.0 METAL2
- 9.1 Minimum Width 3
- 9.2 Minimum Spacing 4
- 9.3 Overlap of VIA 4

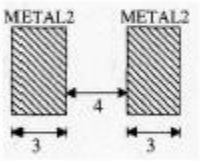


Figure 3.17. SCNA design rules (continued).

values in conjunction with drawings. Some have been omitted or merged for simplicity, but can be accessed by having L-Edit print the complete set. In the drawings, note that the derived layers
N+ = (NSELECT) AND (ACTIVE)
P+ = (PSELECT) AND (ACTIVE)
are equivalent to **ndiff** (n_+) and **pdiff** (p_+) doped regions.

3.8 Latch-Up

Latch-up is a condition that may occur in CMOS integrated circuits where
• The circuits cease to operate;
• There is excessive consumption of current from the power supply, which may cause overheating and chip failure; and,
• The only way to take the chip out of latch-up is to disconnect the power supply.
Latch-up originates from the n and p layers used to create nMOS and pMOS transistors in the CMOS fabrication process. As such, it can be prevented by following certain rules in the layout and electrical connections.
Let us first examine why latch-up occurs. Figure 3.28 shows a basic cross-section of an n-well CMOS chip. Note that the power supply and ground connections have been included. Following the connections from V_{DD} to ground shows the existence of a 4-layer pnpn structure:
p_+ connected to VDD;
n-well;
p-substrate;
n_+ connected to ground.
If the chip goes into latch-up, current flows from the power supply to ground as shown. The circuits do not function since they do not receive any current.
In power electronics, the pnpn layering scheme is used to create a device known as a silicon-controlled rectifier (SCR), which is used as a switched rectifier.The I-characteristics are shown in Figure 3.29. For small voltages, the structure acts like a reverse-biased pn junction, and only leakage current flows. However, if the applied voltage reaches the **break-over voltage** V_{BO}, then the curve exhibits a negative slope. This results in a very quick drop in the voltage accompanied by an increase

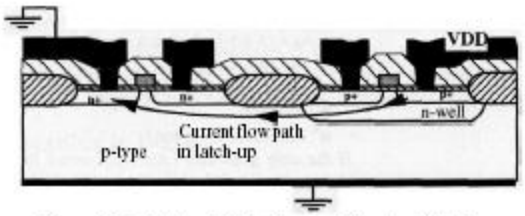
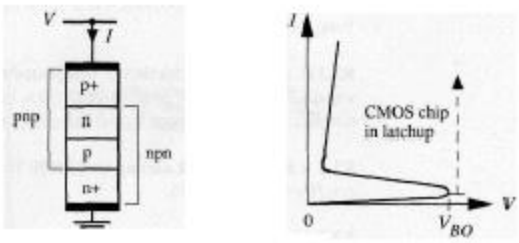


Figure 3.28. Origin of the latch-up problem in CMOS.



(a) 4-layer structure (b) I-V characteristics

Figure 3.29. Four-layer (pnpn) device characteristics.

in the current. In CMOS, this corresponds to the chip going into latch-up.
Latch-up is often explained using bipolar transistor models. The drawing shows that both pnp and npn transistors can be visualized from the layering. Since the two

transistors share the internal n and p layers, they are automatically connected in a feedback loop. Using this viewpoint, latch-up occurs when the sum of the commonbase current gains equals unity:

$$\alpha_{npn} + \alpha_{pnp} = 1. \qquad (3.13)$$

One approach to reducing the occurrence of latchup is to ensure that the gains of the bipolar transistors are kept small by reducing the efficiency of the emitter and base regions.

At the physical design level, latch-up prevention is achieved by adhering to a set of rules that are designed to either distribute the voltages throughout the layered regions, or reduce the current gain of the bipolar transistors. The following items are common to most processes.

• **Use guard rings** around MOSFETs;
• Provide liberal substrate contacts to ground, and n-well contacts to V_{DD};
• Obey all design rules.

Guard rings are p^+ regions connected to ground surrounding nMOSFETs, or n^+ regions connected to V_{DD} surrounding pMOSFETs, that are added to reduce the gains of the parasitic bipolar transistors.

Latch-up prevention techniques are usually specified for a given fabrication process, and should be followed to ensure a functional design.

Design of High Speed CMOS Logic Networks
(Chapter 8 of John.P.Uyemura and Chapter5 of EC74)

In VLSI technology, switching speed of logic circuits is an important parameter and is closely related to the timing specifications. Modern CMOS technology is capable of fabricating MOSFETS with channel lengths smaller than 65 nm. Here, the aspect ratio (W/L) is the important critical parameter in high speed CMOS logic networks.

Gate delays: Gate delay is defined as the time taken by the Logic gate to respond to the signal given at its input. As shown in fig.1, the NAND gate takes a fixed duration to give the output after the input is given. This time is the gate delay. The parameters associated with the gate delay are transistor resistance, Capacitance and the load capacitance, C_L. Fig.2 illustrates the variation of the gate delay for different values of C_L.

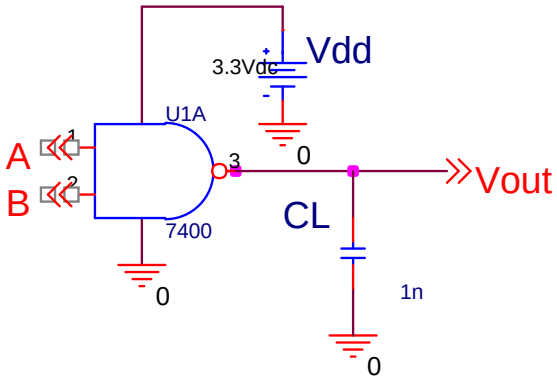


Fig.1 Circuit to illustrate the definition of of gate delay

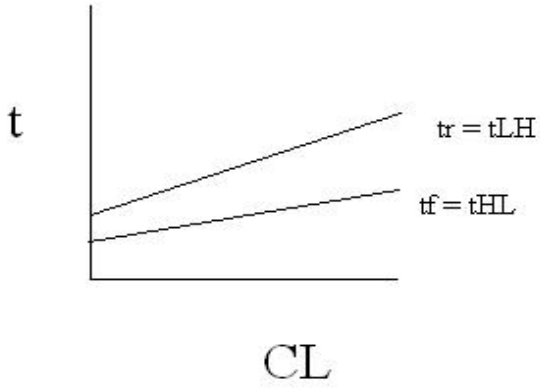
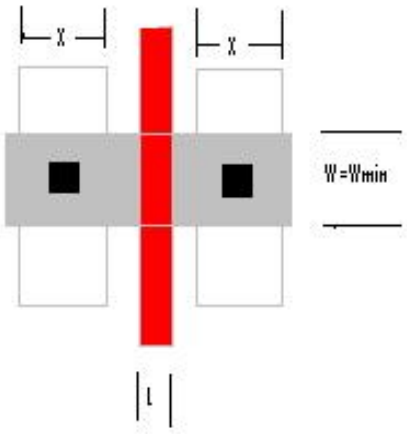


Fig.2 Graph of delay time v/s load capacitance

FET unit Resistance is given by $R_u = \dfrac{1}{k'\left(\dfrac{W}{L}\right)(V_{DD} - V_T)}$

Where Ru is unit transistor Resistance, W and L are the width and Length of the

transistor, K' is «$_n C_{ox}$ $R_m = \dfrac{R_u}{m}, C_{Gm} = mC_{Gu}, C_{Dm} = mC_{Du}, C_{Sm} = mC_{Su}$



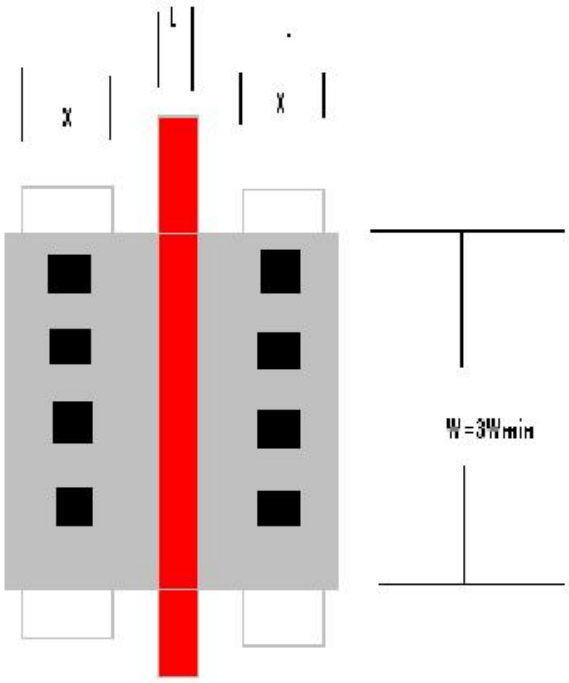


Fig.3 Minimum-Size FET **Fig.4 3X Scaled- FET**

Fig.3 shows the layout of FET and Fig.4 shows the scaled FET, 3 times the original size. The parasitic capacitances for unit size FET are given by

$$C_{Gu} = C_{OX}(WL)_u$$
$$C_{Du} = (C_{GD} + C_{DB})_u$$
$$C_{Su} = (C_{GS} + C_{SB})_u$$

where C_{Gu}, C_{Du} and C_{su} are the Gate, Drain and Source Capacitances. The width of unit size FET is the minimum size given by $W_{min} = W_u$. Fig.4 shows the scaled FET with m = 3. The aspect ratio becomes 3 times the unit FET and the aspect ratio also become e times unit FET. In general, the size of scaled FETs are integer multiples of the minimum

$$(W)_3 = 3W_u \qquad \left(\frac{W}{L}\right)_3 = 3\left(\frac{W}{L}\right)_u$$

The FET parasitic resistance and capacitance becomes

$$R_u = mR_u, C_{Gu} = mC_{Gu}, C_{Du} = mC_{Du}, C_{Su} = mC_{Su}$$

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