Power Electronics






Notes

POWER TRANSISTORS

Power transistors are devices that have controlled turn-on and turn-off characteristics. These devices are used a switching devices and are operated in the saturation region resulting in low on-state voltage drop. They are turned on when a current signal is given to base or control terminal. The transistor remains on so long as the control signal is present. The switching speed of modern transistors is much higher than that of thyristors and are used extensively in dc-dc and dc-ac converters. However their voltage and current ratings are lower than those of thyristors and are therefore used in low to medium power applications.

Power transistors are classified as follows

- Bipolar junction transistors(BJTs)
- Metal-oxide semiconductor filed-effect transistors(MOSFETs)
- Static Induction transistors(SITs)
- Insulated-gate bipolar transistors(IGBTs)

BIPOLAR JUNCTION TRANSISTORS

The need for a large blocking voltage in the off state and a high current carrying capability in the on state means that a power BJT must have substantially different structure than its small signal equivalent. The modified structure leads to significant differences in the I-V characteristics and switching behavior between power transistors and its logic level counterpart.

POWER TRANSISTOR STRUCTURE

If we recall the structure of conventional transistor we see a thin p-layer is sandwiched between two n-layers or vice versa to form a three terminal device with the terminals named as Emitter, Base and Collector.

The structure of a power transistor is as shown below

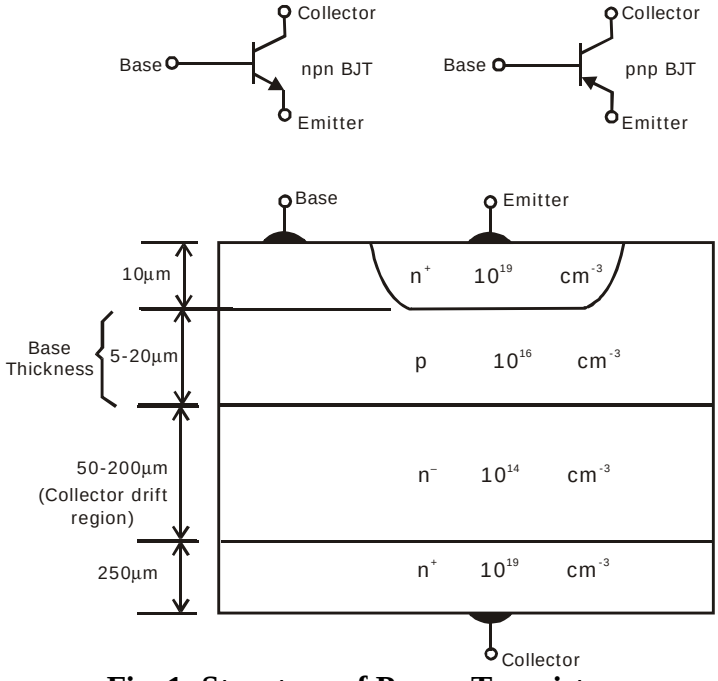


Fig. 1: Structure of Power Transistor

The difference in the two structures is obvious.

A power transistor is a vertically oriented four layer structure of alternating p-type and n-type. The vertical structure is preferred because it maximizes the cross sectional area and through which the current in the device is flowing. This also minimizes on-state resistance and thus power dissipation in the transistor.

The doping of emitter layer and collector layer is quite large typically 10^{19} cm^{-3}. A special layer called the collector drift region (n^-) has a light doping level of 10^{14}.

The thickness of the drift region determines the breakdown voltage of the transistor. The base thickness is made as small as possible in order to have good amplification capabilities, however if the base thickness is small the breakdown voltage capability of the transistor is compromised.

Practical power transistors have their emitters and bases interleaved as narrow fingers as shown. The purpose of this arrangement is to reduce the effects of current crowding. This multiple emitter layout also reduces parasitic ohmic resistance in the base current path which reduces power dissipation in the transistor.

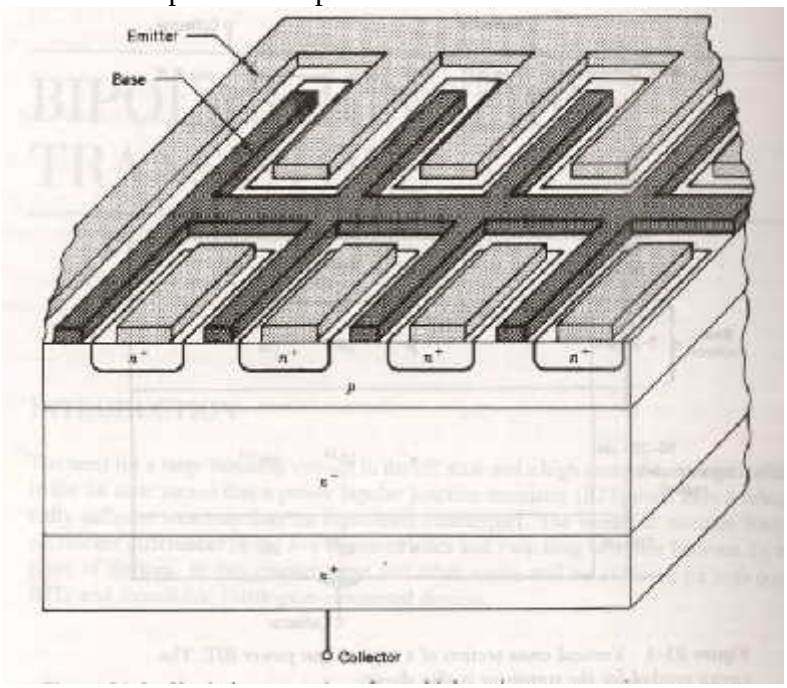


Fig. 2

STEADY STATE CHARACTERISTICS

Figure 3(a) shows the circuit to obtain the steady state characteristics. Fig 3(b) shows the input characteristics of the transistor which is a plot of I_B versus V_{BE}. Fig 3(c) shows the output characteristics of the transistor which is a plot I_C versus V_{CE}. The characteristics shown are that for a signal level transistor.

The power transistor has steady state characteristics almost similar to signal level transistors except that the V-I characteristics has a region of quasi saturation as shown by figure 4.

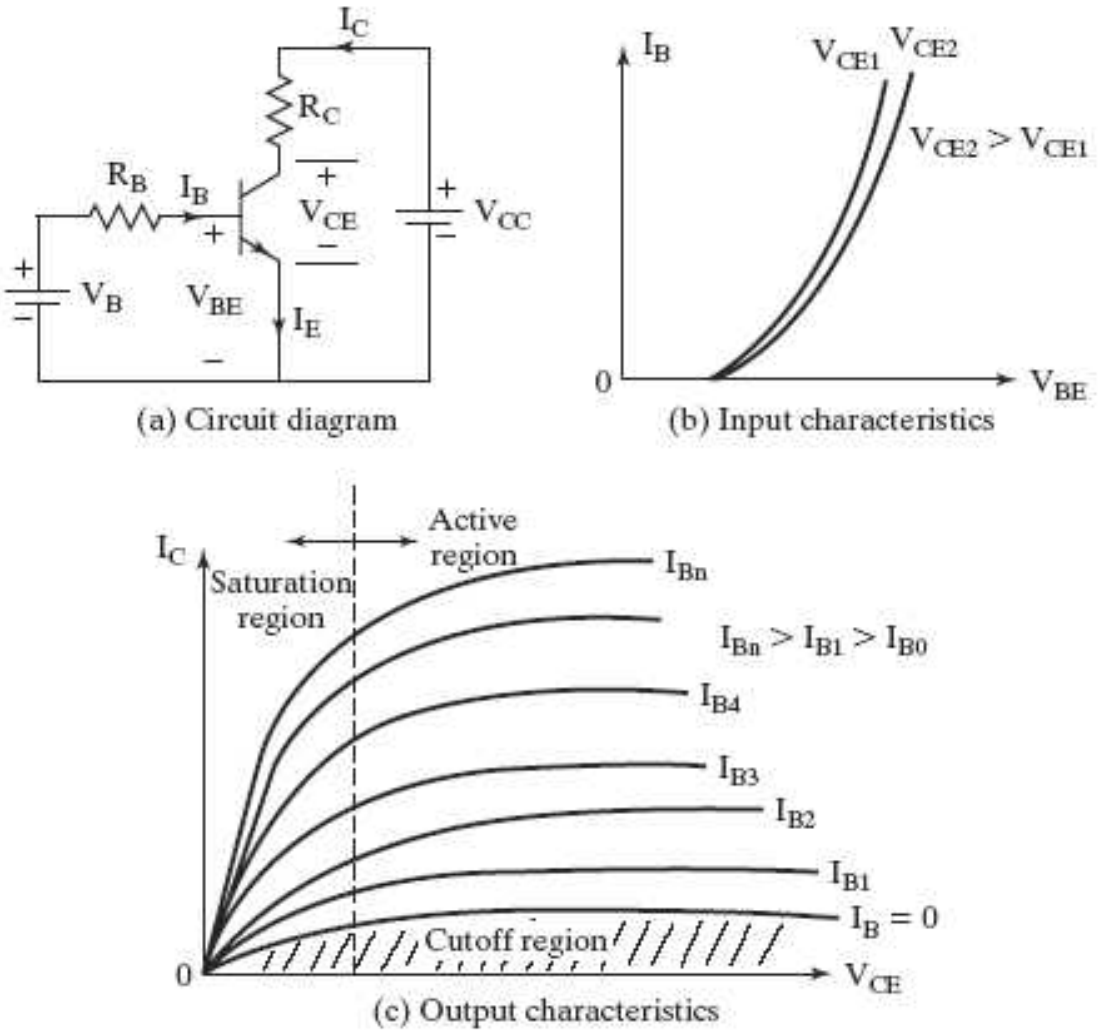


Fig. 3: Characteristics of NPN Transistors

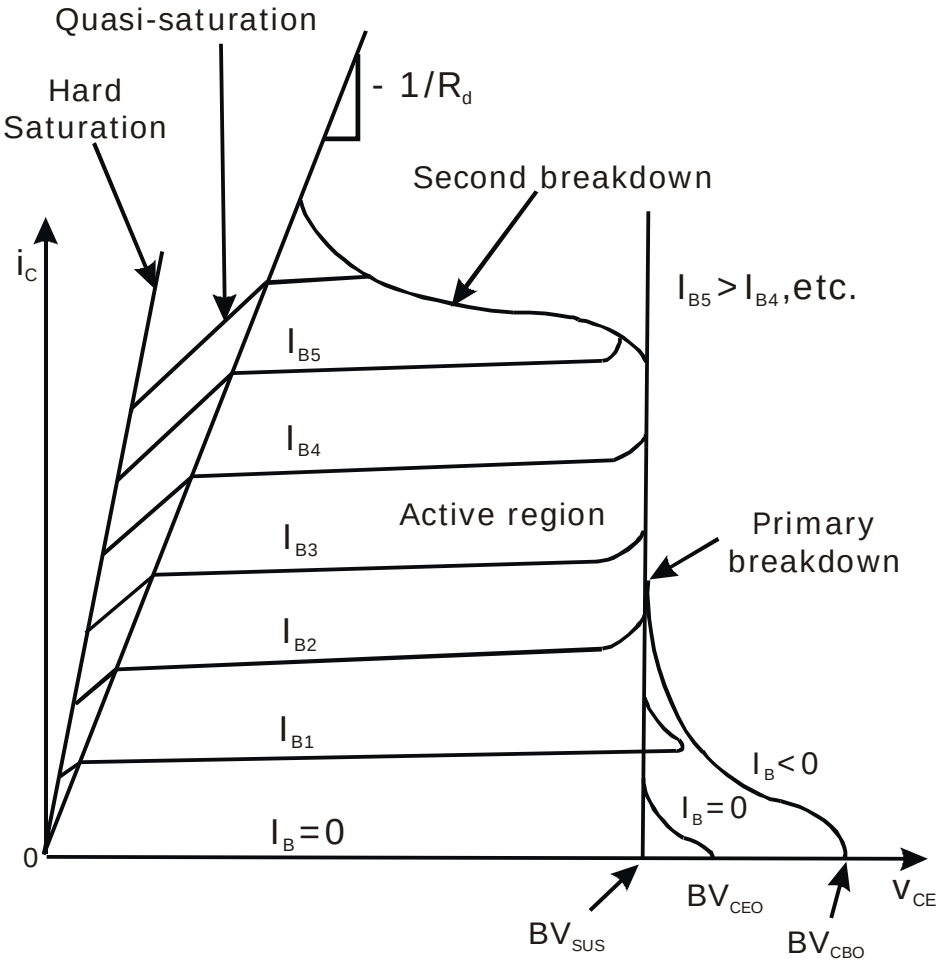


Fig. 4: Characteristics of NPN Power Transistors

There are four regions clearly shown: Cutoff region, Active region, quasi saturation and hard saturation. The cutoff region is the area where base current is almost zero. Hence no collector current flows and transistor is off. In the quasi saturation and hard saturation, the base drive is applied and transistor is said to be on. Hence collector current flows depending upon the load. The power BJT is never operated in the active region (i.e. as an amplifier) it is always operated between cutoff and saturation. The BV_{SUS} is the maximum collector to emitter voltage that can be sustained when BJT is carrying substantial collector current. The BV_{CEO} is the maximum collector to emitter breakdown voltage that can be sustained when base current is zero and BV_{CBO} is the collector base breakdown voltage when the emitter is open circuited.

The primary breakdown shown takes place because of avalanche breakdown of collector base junction. Large power dissipation normally leads to primary breakdown.

The second breakdown shown is due to localized thermal runaway. This is explained in detail later.

TRANSFER CHARACTERISTICS

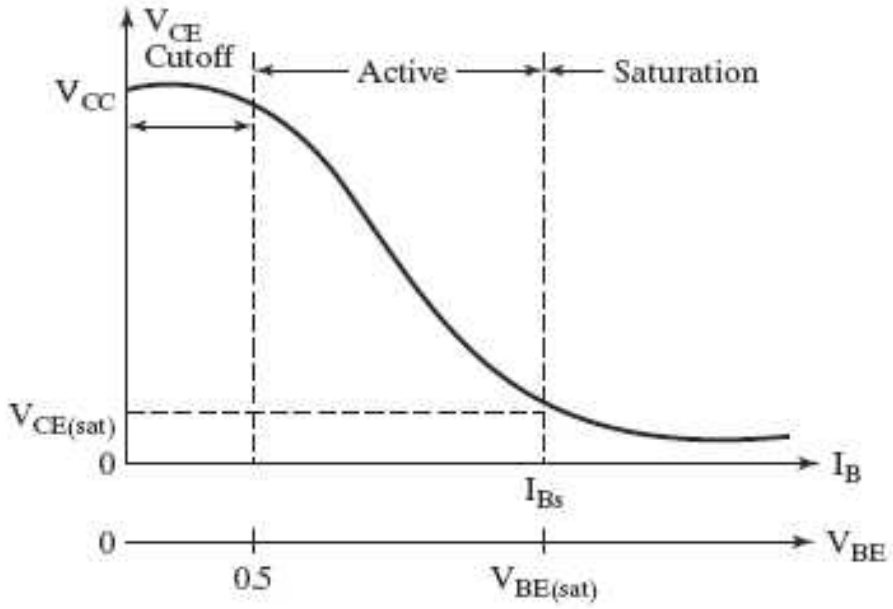


Fig. 5: Transfer Characteristics

$$I_E = I_C + I_B$$

$$= h_{fE} = \frac{I_C}{I_B}$$

$$I_C = \quad I_B + I_{CEO}$$

$$\sim = \frac{\quad}{+1}$$

$$= \frac{\sim}{1-\sim}$$

TRANSISTOR AS A SWITCH

The transistor is used as a switch therefore it is used only between saturation and cutoff. From fig. 5 we can write the following equations

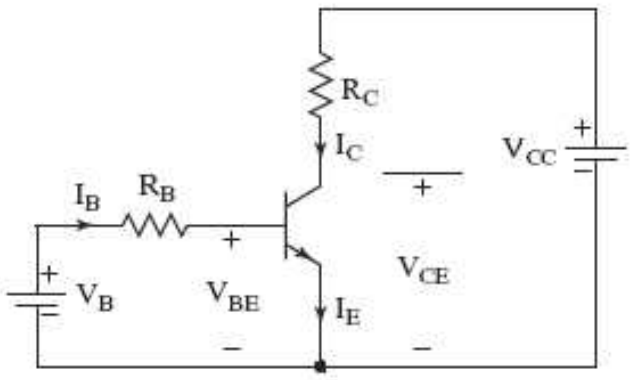


Fig. 6: Transistor Switch

$$I_B = \frac{V_B - V_{BE}}{R_B}$$

$$V_C = V_{CE} = V_{CC} - I_C R_C$$

$$V_C = V_{CC} - \frac{R_C (V_B - V_{BE})}{R_B}$$

$$V_{CE} = V_{CB} + V_{BE}$$

$$V_{CB} = V_{CE} - V_{BE} \qquad ....(1)$$

Equation (1) shows that as long as $V_{CE} > V_{BE}$ the CBJ is reverse biased and transistor is in active region, The maximum collector current in the active region, which can be obtained by setting $V_{CB} = 0$ and $V_{BE} = V_{CE}$ is given as

$$I_{CM} = \frac{V_{CC} - V_{CE}}{R_C} \qquad \therefore \quad I_{BM} = \frac{I_{CM}}{F}$$

If the base current is increased above I_{BM}, V_{BE} increases, the collector current increases and V_{CE} falls below V_{BE}. This continues until the CBJ is forward biased with V_{BC} of about 0.4 to 0.5V, the transistor than goes into saturation. The transistor saturation may be defined as the point above which any increase in the base current does not increase the collector current significantly.

In saturation, the collector current remains almost constant. If the collector emitter voltage is $V_{CE(sat)}$ the collector current is

$$I_{CS} = \frac{V_{CC} - V_{CESAT}}{R_C}$$

$$I_{BS} = \frac{I_{CS}}{}$$

Normally the circuit is designed so that I_B is higher that I_{BS}. The ratio of I_B to I_{BS} is called to overdrive factor ODF.

$$ODF = \frac{I_B}{I_{BS}}$$

The ratio of I_{CS} to I_B is called as forced .

$$_{forced} = \frac{I_{CS}}{I_B}$$

The total power loss in the two functions is

$$P_T = V_{BE} I_B + V_{CE} I_C$$

A high value of ODF cannot reduce the CE voltage significantly. However V_{BE} increases due to increased base current resulting in increased power loss. Once the transistor is saturated, the CE voltage is not reduced in relation to increase in base current. However the power is increased at a high value of ODF, the transistor may be damaged due to thermal runaway. On the other hand if the transistor is under driven $(I_B < I_{BS})$ it may operate in active region, V_{CE} increases resulting in increased power loss.

PROBLEMS

1. The BJT is specified to have a range of 8 to 40. The load resistance in $R_e = 11\Omega$. The dc supply voltage is V_{CC}=200V and the input voltage to the base circuit is V_B=10V. If $V_{CE(sat)}$=1.0V and $V_{BE(sat)}$=1.5V. Find
   a. The value of R_B that results in saturation with a overdrive factor of 5.
   b. The forced $_f$.
   c. The power loss P_T in the transistor.

Solution

(a) $$I_{CS} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{200 - 1.0}{11\Omega} = 18.1A$$

Therefore $$I_{BS} = \frac{I_{CS}}{\min} = \frac{18.1}{8} = 2.2625A$$

Therefore $$I_B = ODF \times I_{BS} = 11.3125A$$

$$I_B = \frac{V_B - V_{BE(sat)}}{R_B}$$

Therefore $$R_B = \frac{V_B - V_{BE(sat)}}{I_B} = \frac{10 - 1.5}{11.3125} = 0.715\Omega$$

(b) Therefore $$_f = \frac{I_{CS}}{I_B} = \frac{18.1}{11.3125} = 1.6$$

$$P_T = V_{BE} I_B + V_{CE} I_C$$

(c) $$P_T = 1.5 \times 11.3125 + 1.0 \times 18.1$$

$$P_T = 16.97 + 18.1 = 35.07W$$

2. The of a bipolar transistor varies from 12 to 75. The load resistance is $R_C = 1.5\Omega$. The dc supply voltage is V_{CC}=40V and the input voltage base circuit is V_B=6V. If $V_{CE(sat)}$=1.2V, $V_{BE(sat)}$=1.6V and R_B=0.7Ω determine
   a. The overdrive factor ODF.
   b. The forced β_f.
   c. Power loss in transistor P_T

Solution

$$I_{CS} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{40 - 1.2}{1.5} = 25.86A$$

$$I_{BS} = \frac{I_{CS}}{\min} = \frac{25.86}{12} = 2.15A$$

Also $$I_B = \frac{V_B - V_{BE(sat)}}{R_B} = \frac{6 - 1.6}{0.7} = 6.28A$$

(a) Therefore $$ODF = \frac{I_B}{I_{BS}} = \frac{6.28}{2.15} = 2.92$$

Forced $$_f = \frac{I_{CS}}{I_B} = \frac{25.86}{6.28} = 4.11$$

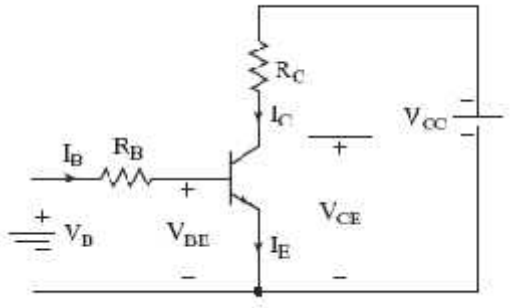
(c) $P_T = V_{BE} I_B + V_{CE} I_C$

$P_T = 1.6 \times 6.25 \; + \; 1.2 \times 25.86$

$P_T = 41.032 Watts$

(JULY / AUGUST 2004)

3. For the transistor switch as shown in figure
   a. Calculate forced beta, $_f$ of transistor.
   b. If the manufacturers specified is in the range of 8 to 40, calculate the minimum overdrive factor (ODF).
   c. Obtain power loss P_T in the transistor.



$V_B = 10V, \quad R_B = 0.75\Omega,$

$V_{BE(sat)} = 1.5V, \; R_C = 11\Omega,$

$V_{CE(sat)} = 1V, \quad V_{CC} = 200V$

Solution

(i) $I_B = \dfrac{V_B - V_{BE(sat)}}{R_B} = \dfrac{10 - 1.5}{0.75} = 11.33A$

$I_{CS} = \dfrac{V_{CC} - V_{CE(sat)}}{R_C} = \dfrac{200 - 1.0}{11} = 18.09A$

Therefore $I_{BS} = \dfrac{I_{CS}}{_{\min}} = \dfrac{18.09}{8} = 2.26A$

$_f = \dfrac{I_{CS}}{I_B} = \dfrac{18.09}{11.33} = 1.6$

(ii) $ODF = \dfrac{I_B}{I_{BS}} = \dfrac{11.33}{2.26} = 5.01$

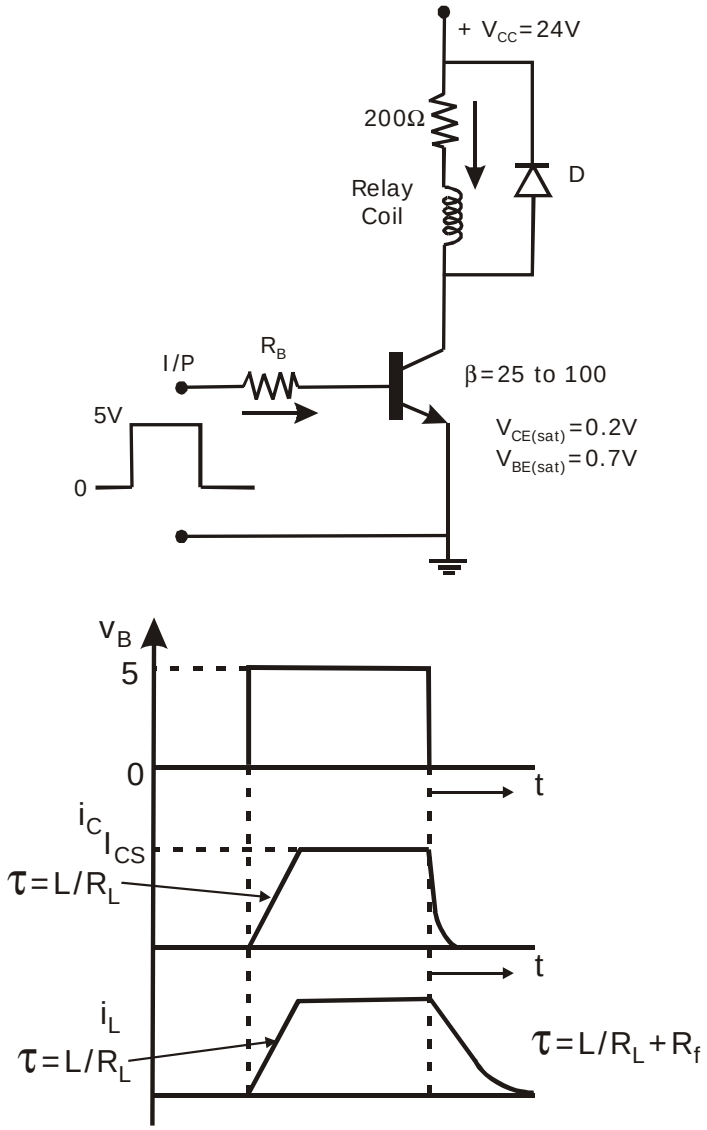
(iii) $P_T = V_{BE} I_B + V_{CE} I_C = 1.5 \times 11.33 + 1.0 \times 18.09 = 35.085W$

(JAN / FEB 2005)

4. A simple transistor switch is used to connect a 24V DC supply across a relay coil, which has a DC resistance of 200Ω. An input pulse of 0 to 5V amplitude is applied through series base resistor R_B at the base so as to turn on the transistor switch. Sketch the device current waveform with reference to the input pulse.

Calculate

a. I_{CS} .
b. Value of resistor R_B , required to obtain over drive factor of two.
c. Total power dissipation in the transistor that occurs during the saturation state.



Solution

To sketch the device current waveforms; current through the device cannot rise fast to the saturating level of I_{CS} since the inductive nature of the coil opposes any change in current through it. Rate of rise of collector current can be determined by the time constant $\tau_1 = \frac{L}{R}$. Where L is inductive in Henry of coil and R is resistance of coil. Once steady state value of I_{CS} is reached the coil acts as a short circuit. The collector current stays put at I_{CS} till the base pulse is present.

Similarly once input pulse drops to zero, the current I_C does not fall to zero immediately since inductor will now act as a current source. This current will

now decay at the fall to zero. Also the current has an alternate path and now can flow through the diode.

(i) $$I_{CS} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{24 - 0.2}{200} = 0.119A$$

(ii) Value of R_B

$$I_{BS} = \frac{I_{CS}}{\min} = \frac{0.119}{25} = 4.76mA$$

$$\therefore \quad I_B = ODF \times I_{BS} = 2 \times 4.76 = 9.52mA$$

$$\therefore \quad R_B = \frac{V_B - V_{BE(sat)}}{I_B} = \frac{5 - 0.7}{9.52} = 450\Omega$$

(iii) $$P_T = V_{BE(sat)} \times I_B + V_{CE(sat)} \times I_{CS} = 0.7 \times 9.52 + 0.2 \times 0.119 = 6.68W$$

SWITCHING CHARACTERISTICS

A forward biased p-n junction exhibits two parallel capacitances; a depletion layer capacitance and a diffusion capacitance. On the other hand, a reverse biased p-n junction has only depletion capacitance. Under steady state the capacitances do not play any role. However under transient conditions, they influence turn-on and turn-off behavior of the transistor.

TRANSIENT MODEL OF BJT

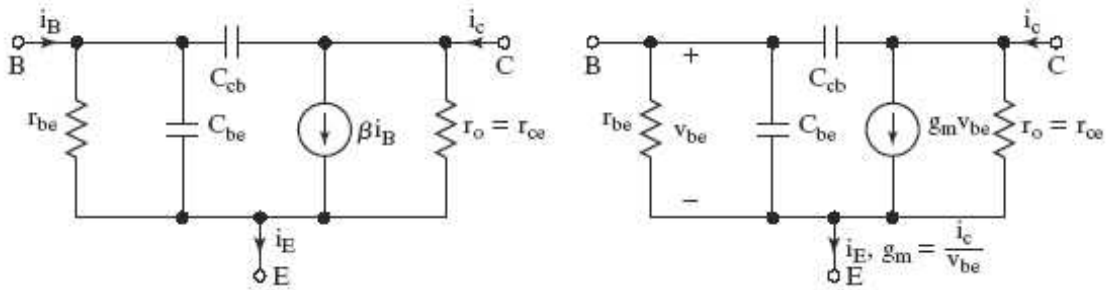


Fig. 7: Transient Model of BJT

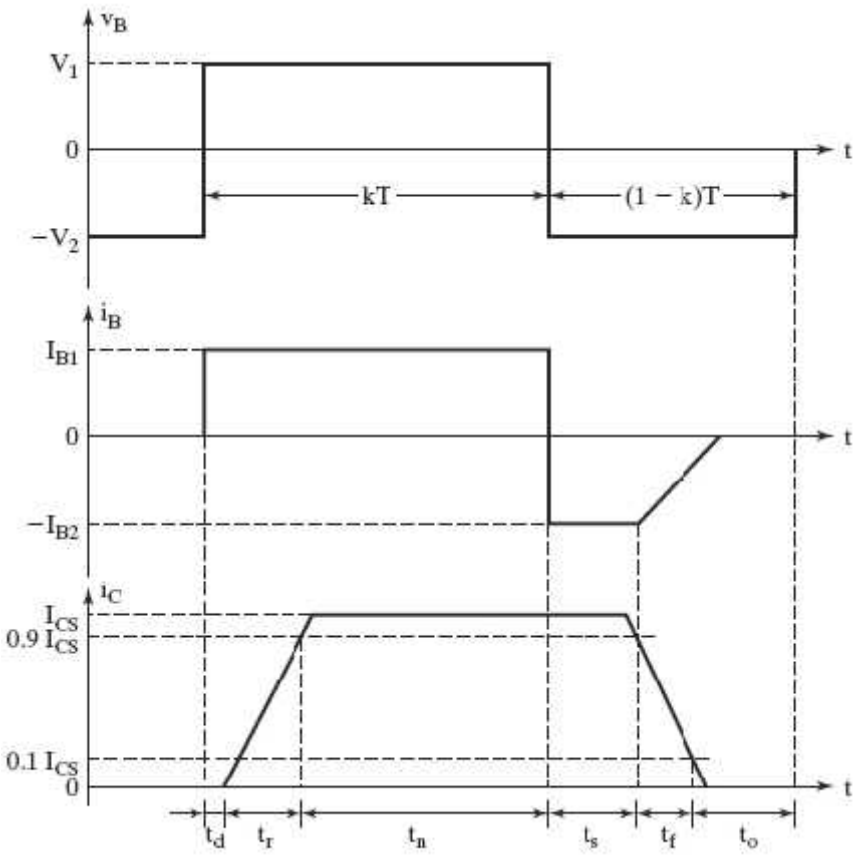


Fig. 8: Switching Times of BJT

Due to internal capacitances, the transistor does not turn on instantly. As the voltage V_B rises from zero to V_1 and the base current rises to I_{B1}, the collector current does not respond immediately. There is a delay known as delay time td, before any collector current flows. The delay is due to the time required to charge up the BEJ to the forward bias voltage V_{BE}(0.7V). The collector current rises to the steady value of I_{CS} and this time is called rise time t_r.

The base current is normally more than that required to saturate the transistor. As a result excess minority carrier charge is stored in the base region. The higher the ODF, the greater is the amount of extra charge stored in the base. This extra charge which is called the saturating charge is proportional to the excess base drive.

This extra charge which is called the saturating charge, is proportional to the excess base drive and the corresponding current I_e.

$$I_e = I_B - \frac{I_{CS}}{} = ODF.I_{BS} - I_{BS} = I_{BS}\left(ODF - 1\right)$$

Saturating charge $Q_S = \tau_s I_e = \tau_s I_{BS}(ODF - 1)$ where τ_s is known as the storage time constant.

When the input voltage is reversed from V_1 to $-V_2$, the reverse current $-I_{B2}$ helps to discharge the base. Without $-I_{B2}$ the saturating charge has to be removed entirely due to recombination and the storage time t_s would be longer.

Once the extra charge is removed, BEJ charges to the input voltage $-V_2$ and the base current falls to zero. t_f depends on the time constant which is determined by the reverse biased BEJ capacitance.

$$\therefore \qquad t_{on} = t_d + t_r$$
$$t_{off} = t_s + t_f$$

PROBLEMS

1. For a power transistor, typical switching waveforms are shown. The various parameters of the transistor circuit are as under $V_{cc} = 220V$, $V_{CE(sat)} = 2V$, $I_{CS} = 80A$, $td = 0.4\mu s$, $t_r = 1\mu s$, $t_n = 50\mu s$, $t_s = 3\mu s$, $t_f = 2\mu s$, $t_0 = 40\mu s$, $f = 5Khz$, $I_{CEO} = 2mA$. Determine average power loss due to collector current during t_{on} and t_n. Find also the peak instantaneous power loss, due to collector current during turn-on time.

Solution

During delay time, the time limits are $0 \le t \le td$. Figure shows that in this time $i_c(t) = I_{CEO}$ and $V_{CE}(t) = V_{CC}$. Therefore instantaneous power loss during delay time is $P_d(t) = i_C V_{CE} = I_{CEO} V_{CC} = 2x10^{-3} x220 = 0.44W$

Average power loss during delay time $0 \le t \le td$ is given by

$$Pd = \frac{1}{T}\int_0^{td} i_c(t)\, v_{CE}(t)\, dt$$

$$Pd = \frac{1}{T}\int_0^{td} I_{CEO} V_{CC}\, dt$$

$$Pd = f.I_{CEO} V_{CC} td$$

$$Pd = 5x10^3 \times 2\times10^{-3} \times 220 \times 0.4 \times 10^{-6} = 0.88mW$$

During rise time $0 \le t \le t_r$

$$i_c(t) = \frac{I_{CS}}{t_r} t$$

$$v_{CE}(t) = \left[V_{CC} - \left(\frac{V_{CC} - V_{CE(sat)}}{t_r} \right) t \right]$$

$$v_{CE}(t) = V_{CC} + \left[V_{CE(sat)} - V_{CC} \right] \frac{t}{t_r}$$

Therefore average power loss during rise time is

$$P_r = \frac{1}{T}\int_0^{t_r} \frac{I_{CS}}{t_r} t \left[V_{CC} + \left(V_{CE(sat)} - V_{CC} \right) \frac{t}{t_r} \right] dt$$

$$P_r = f.I_{CS} t_r \left[\frac{V_{CC}}{2} - \frac{V_{CC} - V_{CES}}{3} \right]$$

$$P_r = 5x10^3 \times 80 \times 1 \times 10^{-6} \left[\frac{220}{2} - \frac{220-2}{3} \right] = 14.933W$$

Instantaneous power loss during rise time is

$$P_r(t) = \frac{I_{CS}}{t_r} t \left[V_{CC} - \frac{V_{CC} - V_{CE}(sat)}{t_r} t \right]$$

$$P_r(t) = \frac{I_{CS}}{t_r} t V_{CC} - \frac{I_{CSt}^{\ 2}}{t_r^{\ 2}} \left[V_{CC} - V_{CE(sat)} \right]$$

Differentiating the above equation and equating it to zero will give the time t_m at which instantaneous power loss during t_r would be maximum.

Therefore $$\frac{dP_r(t)}{dt} = \frac{I_{CS} V_{CC}}{t_r} - \frac{I_{CS}\, 2t}{t_r^{\ 2}} [V_{CC} - V_{CEsat}]$$

At $t = t_m$, $$\frac{dP_r(t)}{dt} = 0$$

Therefore $$0 = \frac{I_{CS}}{t_r} V_{CC} - \frac{2 I_{CS} t_m}{t_r^{\ 2}} \left[V_{CC} - V_{CE(sat)} \right]$$

$$\frac{\not{I}_{CS}}{\not{t}_r} V_{cc} = \frac{2 \not{I}_{CS} t_m}{\not{t}_r^{\ 2}} \left[V_{CC} - V_{CE(sat)} \right]$$

$$\frac{t_r V_{CC}}{2} = t_m \left[V_{CC} - V_{CE(sat)} \right]$$

Therefore $$t_m = \frac{t_r V_{CC}}{2 \left[V_{CC} - V_{CE(sat)} \right]}$$

Therefore $$t_m = \frac{V_{CC} t_r}{2 \left[V_{CC} - V_{CE(sat)} \right]} = \frac{220 \times 1 \times 10^{-6}}{2[200 - 2]} = 0.5046 « s$$

Peak instantaneous power loss P_{rm} during rise time is obtained by substituting the value of t=tm in equation (1) we get

$$P_{rm} = \frac{I_{CS}}{t_r} \frac{V_{CC}^{\ 2} t_r}{2 \left[V_{CC} - V_{CE(sat)} \right]} - \frac{I_{CS}}{t_r^{\ 2}} \frac{\left(V_{CC} t_r \right)^2 \left[V_{CC} - V_{CE(sat)} \right]}{4 \left[V_{CC} - V_{CE(sat)} \right]^2}$$

$$P_{rm} = \frac{80 \times 220^2}{4[220 - 2]} = 4440.4W$$

Total average power loss during turn-on

$$P_{on} = Pd + P_r = 0.00088 + 14.933 = 14.9339W$$

During conduction time $0 \le t \le t_n$

$$i_C(t) = I_{CS} \;\&\; v_{CE}(t) = V_{CE(sat)}$$

Instantaneous power loss during t_n is

$$P_n(t) = i_C v_{CE} = I_{CS} V_{CE(sat)} = 80 \; x \; 2 = 160W$$

Average power loss during conduction period is

$$P_n = \frac{1}{T} \int_0^{t_n} i_C v_{CE} dt = f I_{CS} V_{CES} t_n = 5 \times 10^3 \times 80 \times 2 \times 50 \times 10^{-6} = 40W$$

PERFORMANCE PARAMETERS

DC gain $h_{FE} = \frac{I_C}{I_B}[V_{CE}]$: Gain is dependent on temperature. A high gain would reduce the values of forced $\& V_{CE(sat)}$.

$V_{CE(sat)}$: A low value of $V_{CE(sat)}$ will reduce the on-state losses. $V_{CE(sat)}$ is a function of the collector circuit, base current, current gain and junction temperature. A small value of forced β decreases the value of $V_{CE(sat)}$.

$V_{BE(sat)}$**:** A low value of $V_{BE(sat)}$ will decrease the power loss in the base emitter junction. $V_{BE(sat)}$ increases with collector current and forced β.

Turn-on time t_{on}**:** The turn-on time can be decreased by increasing the base drive for a fixed value of collector current. t_d is dependent on input capacitance does not change significantly with I_C. However t_r increases with increase in I_C.

Turn off time t_{off}: The storage time t_s is dependent on over drive factor and does not change significantly with I_C. t_f is a function of capacitance and increases with I_C. $t_s \& t_f$ can be reduced by providing negative base drive during turn-off. t_f is less sensitive to negative base drive.

Cross-over t_C**:** The crossover time t_C is defined as the interval during which the collector voltage V_{CE} rises from 10% of its peak off state value and collector current. I_C falls to 10% of its on-state value. t_C is a function of collector current negative base drive.

Switching Limits

SECOND BREAKDOWN

It is a destructive phenomenon that results from the current flow to a small portion of the base, producing localized hot spots. If the energy in these hot spots is sufficient the excessive localized heating may damage the transistor. Thus secondary breakdown is caused by a localized thermal runaway. The SB occurs at certain combinations of voltage, current and time. Since time is involved, the secondary breakdown is basically an energy dependent phenomenon.

FORWARD BIASED SAFE OPERATING AREA FBSOA

During turn-on and on-state conditions, the average junction temperature and second breakdown limit the power handling capability of a transistor. The manufacturer usually provide the FBSOA curves under specified test conditions. FBSOA indicates the $I_c - V_{ce}$ limits of the transistor and for reliable operation the transistor must not be subjected to greater power dissipation than that shown by the FBSOA curve.

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